L Number	Hits	Search Text	DB	Time stamp
1	0	fe72al11o17	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 15:55
2	26	fealo	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 15:56
3	47	magnetic adj loss and semiconductor and die	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 15:58
4	12491	tokin.as.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 15:59
5	12	semiconductor adj wafer and magnetic adj loss	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 15:59
6	14	semiconductor adj wafer and tokin.as.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:01
7	2	("3963489").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:03
8	19	3963489.URPN.	USPAT	2004/05/24 16:05
9	19	3963489.uref.	USPAT	2004/05/24 16:08
10	26	semiconductor adj die and magnetic adj material	USPAT	2004/05/24 16:16
11	22	5138431.URPN.	USPAT	2004/05/24 16:14
12	4	noise adj suppression and tokin.as.	USPAT	2004/05/24 16:16

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	0	fe72a11o17	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:47
2	BRS	L2	26	fealo	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:52
3	BRS	L3	47	magnetic adj loss and semiconductor and die	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:53
4	BRS	L4	12491	tokin.as.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:53
5	BRS	L5	12	semiconductor adj wafer and magnetic adj loss	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:53

	Type	L #	Hits	Search Text	DBs	Time Stamp
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7	BRS	L7	19	3963489.uref.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:53
8	BRS	L8	43	semiconductor adj die and magnetic adj material	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:54
9	BRS	L9	25	noise adj suppression and tokin.as.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 16:54

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	4236	bare adj chip	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:39
2	BRS	L2	747995	(integrated adj circuit) or IC	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:49
3	BRS	L3	237350	(back adj surface) or (back adj side)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:40
4	BRS	L4	1932	magnetic adj loss	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:40
5	BRS	L5	1962035	substrate or wafer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:40

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8	BRS	L8	1	6 same 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:42
9	BRS	L9	1	6 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:42
10	BRS	L10	1251673	magnetic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:42

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12	BRS	L12	91811	magnetic near4 (fe or co or ni or f or n or o or cobalt or nickle or iron or fluorine or nitrogen or oxygen)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:46
13	BRS	L13	1	1 near8 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:47
14	BRS	L14	2	1 same 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:49
15	BRS	L15	1580908	(integrated adj circuit) or IC or chip or die or dice	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:49

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16	BRS	L16	49109	10 same 15	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:56
17	BRS	L17	1393	12 same 15	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:57
18	BRS	L19	0	18 same 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 13:58
19	BRS	L18	225	17 same 5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 14:57
20	BRS	L20	13	18 and 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 14:07

	Type	L #	Hits	Search Text	DBs	Time Stamp
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23	BRS	L23	0	21 near16 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 14:57
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25	BRS	L25	40	3 same 5 same 2 same 10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 15:01

US006653573B2

(12) **United States Patent**
Awakura et al.

(10) **Patent No.: US 6,653,573 B2**
(45) **Date of Patent: Nov. 25, 2003**

(54) **WIRING BOARD COMPRISING GRANULAR MAGNETIC FILM**

(75) Inventors: **Yoshio Awakura**, Yokohama (JP); **Shinya Watanabe**, Tokyo (JP); **Satoshi Shiratori**, Tokyo (JP); **Hiroshi Ono**, Yokohama (JP)

(73) Assignee: **NEC Tokin Corporation**, Miyagi (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/825,418**

(22) Filed: **Apr. 3, 2001**

(65) **Prior Publication Data**

US 2001/0037897 A1 Nov. 8, 2001

(30) **Foreign Application Priority Data**

Apr. 4, 2000 (JP) 2000-101756
Apr. 4, 2000 (JP) 2000-101765

(51) **Int. Cl.**[7] **H05K 1/03**; H05K 1/09

(52) **U.S. Cl.** **174/256**; 174/258; 174/260; 361/816; 257/659

(58) **Field of Search** 174/254–256, 174/258–261, 257; 361/793–795, 816, 818, 762, 777; 257/659–661

(56) **References Cited**

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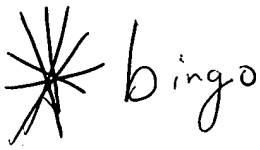
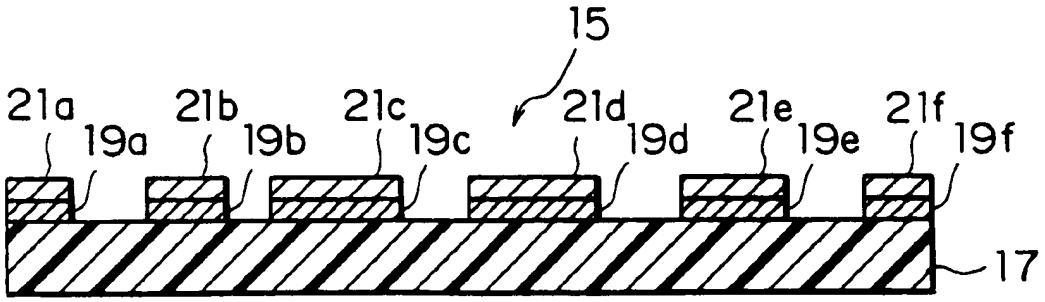


Primary Examiner—Kamand Cuneo
Assistant Examiner—Tuan Dinh
(74) *Attorney, Agent, or Firm*—Bradley N Ruben, PC

(57) **ABSTRACT**

In order to provide a wiring board comprising a magnetic material effective in suppressing spurious radiation in semiconductor devices and electronic circuits and the like that operate at high speeds, a wiring board (**15**) comprises an insulative base material (**17**), conductor patterns (**19***a* to **19***f*) formed thereon, and magnetic thin films (**21***a* to **21***f*) formed on the conductor patterns (**19***a* to **19***f*). The magnetic thin film is configured of a magnetic loss material represented by M—X—Y, where M is at least one of Fe, Co, and Ni, X is at least one element other than M or Y, and Y is at least one of F, N, and O, the maximum value μ"max of the loss factor μ" that is an imaginary component in the complex permeability characteristic of the magnetic loss material exists within a frequency range of 100 MHz to 10 GHz, and a relative bandwidth bwr is not greater than 200% or not smaller than 150% where the relative bandwidth bwr is obtained by extracting a frequency bandwidth between two frequencies at which the value of μ" is 50% of the maximum $\mu"_{max}$ and normalizing the frequency bandwidth at the center frequency thereof.

33 Claims, 10 Drawing Sheets



US006719615B1

(12) **United States Patent**
Molnar

(10) **Patent No.: US 6,719,615 B1**
(45) **Date of Patent: Apr. 13, 2004**

(54) **VERSATILE WAFER REFINING**

(75) Inventor: **Charles J. Molnar**, Wilmington, DE (US)

(73) Assignee: **Beaver Creek Concepts Inc**, Wilmington, DE (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/218,740**

(22) Filed: **Aug. 14, 2002**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/974,129, filed on Oct. 9, 2001, now Pat. No. 6,435,948.

(60) Provisional application No. 60/396,264, filed on Jul. 16, 2002, provisional application No. 60/389,042, filed on Jun. 14, 2002, provisional application No. 60/386,567, filed on Jun. 6, 2002, provisional application No. 60/245,121, filed on Nov. 2, 2000, and provisional application No. 60/238,968, filed on Oct. 10, 2000.

(51) **Int. Cl.**[7] **B24B 1/00**

(52) **U.S. Cl.** **451/41**; 451/28; 451/262; 451/288

(58) **Field of Search** 451/41, 11, 28, 451/36, 57, 158, 162, 259, 262, 265, 273, 287, 288, 392, 393, 397, 908; 156/345.1, 345.11, 345.23, 345.51, 345.54, 345.55

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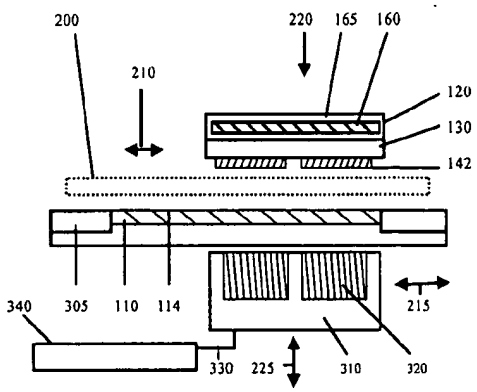
(List continued on next page.)

Primary Examiner—Joseph J. Hail, III
Assistant Examiner—David B. Thomas

(57) **ABSTRACT**

A refining apparatus having magnetically responsive refining elements that can be smaller than the workpiece being refined are disclosed. The refining apparatus can supply a parallel refining motion to the refining element(s) through magnetic coupling forces. The refining apparatus can supply multiple different parallel refining motions to multiple different refining elements solely through magnetic coupling forces to improve refining quality and versatility. New refining methods, refining apparatus, and refining elements disclosed. Methods of refining using frictional refining, chemical refining, tribocbemical refining, and electrochemical refining and combinations thereof are disclosed. A refining chamber can be used. New methods of control are refining disclosed. The new magnetic refining methods, apparatus, and magnetically responsive refining elements can help improve yield and lower the cost of manufacture for refining of workpieces having extremely close tolerances such as semiconductor wafers. Refining fluids are preferred. Reactive refining aids are preferred. Electro-refining for adding and removing material is disclosed. New methods and new apparatus for non-steady state refining control are disclosed.

50 Claims, 27 Drawing Sheets



US006515352B1

(12) **United States Patent**
Spielberger et al.

(10) **Patent No.: US 6,515,352 B1**
(45) **Date of Patent: Feb. 4, 2003**

(54) **SHIELDING ARRANGEMENT TO PROTECT A CIRCUIT FROM STRAY MAGNETIC FIELDS**

(75) Inventors: **Richard K. Spielberger**, Maple Grove, MN (US); **Romney R. Katti**, Maple Grove, MN (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 107 days.

(21) Appl. No.: **09/668,922**

(22) Filed: **Sep. 25, 2000**

(51) **Int. Cl.**[7] **H01L 23/552**
(52) **U.S. Cl.** **257/659**; 257/660
(58) **Field of Search** 257/659, 660

(56) **References Cited**

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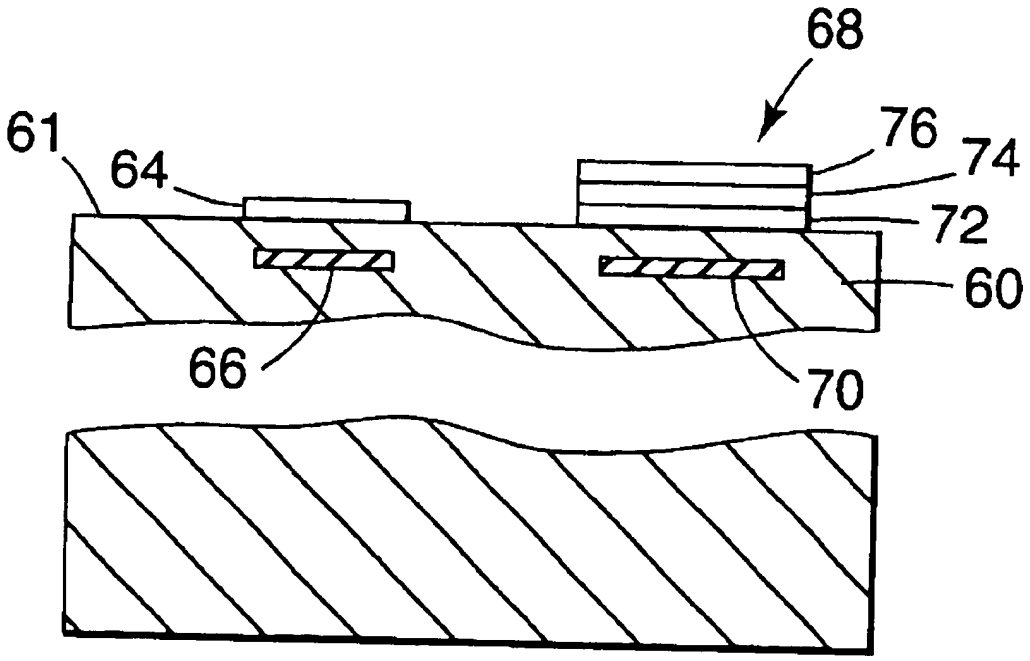
Primary Examiner—Hoai Ho
Assistant Examiner—Andy Huynh
(74) *Attorney, Agent, or Firm*—Knobbe, Martens, Olson & Bear, LLP

(57) **ABSTRACT**

A shielding arrangement for protecting a circuit containing magnetically sensitive materials from external stray magnetic fields. A shield of a material having a relatively high permeability is formed over the magnetically sensitive materials using thin film deposition techniques. Alternatively, a planar shield is affixed directly to a surface of semiconductor die containing an integrated circuit structure.

17 Claims, 2 Drawing Sheets



US006452253B1

(12) **United States Patent**
Tuttle

(10) **Patent No.: US 6,452,253 B1**
(45) **Date of Patent: Sep. 17, 2002**

(54) **METHOD AND APPARATUS FOR MAGNETIC SHIELDING OF AN INTEGRATED CIRCUIT**

(75) Inventor: **Mark Tuttle**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/651,997**

(22) Filed: **Aug. 31, 2000**

(51) **Int. Cl.**[7] **H05K 1/00**
(52) **U.S. Cl.** **257/659**; 257/687
(58) **Field of Search** 257/660, 659, 257/921, 687

(56) **References Cited**

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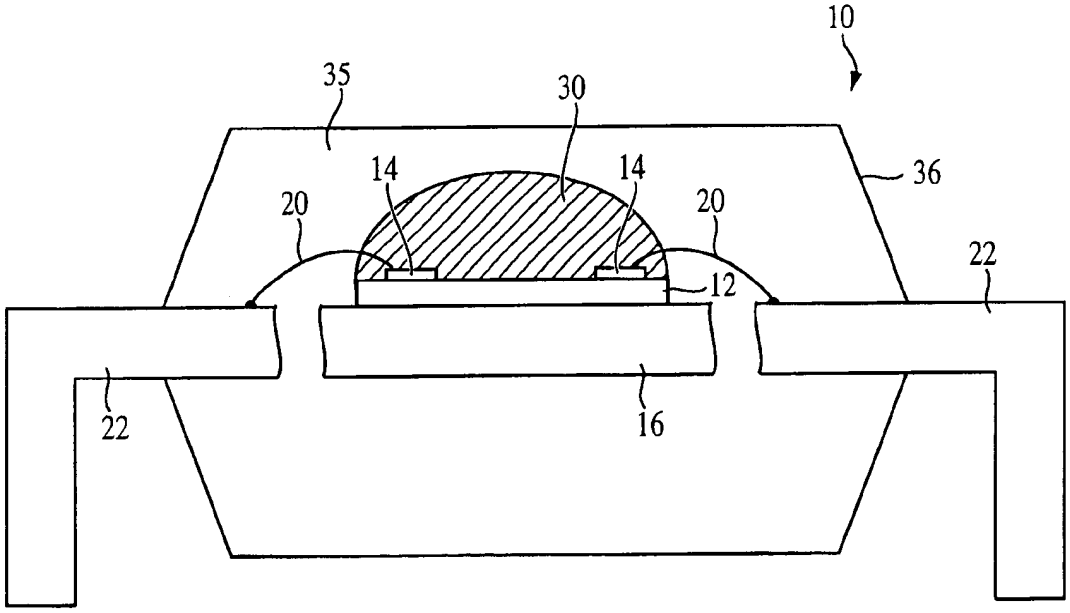
Primary Examiner—Roy Potter
(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

Disclosed are a method and apparatus which provide a magnetic shield for integrated circuits containing electromagnetic circuit elements. The shield is formed of a magnetically permeable material, which may be a nonconductive magnetic oxide, and either partially contacts or completely surrounds the integrated circuit.

33 Claims, 3 Drawing Sheets



US005639989A

United States Patent [19]

Higgins, III

[11] Patent Number: 5,639,989

[45] Date of Patent: Jun. 17, 1997

[54] **SHIELDED ELECTRONIC COMPONENT ASSEMBLY AND METHOD FOR MAKING THE SAME**

[75] Inventor: **Leo M. Higgins, III**, Austin, Tex.

[73] Assignee: **Motorola Inc.**, Schaumburg, Ill.

[21] Appl. No.: **229,495**

[22] Filed: **Apr. 19, 1994**

[51] **Int. Cl.**[6] **H05K 1/00**

[52] **U.S. Cl.** ..... **174/35 MS**; 174/35 R; 361/816; 361/818; 257/655; 257/660

[58] **Field of Search** ..... 174/35 R, 260, 174/35 MS; 361/816, 818; 257/655, 660, 728, 659

[56] **References Cited**

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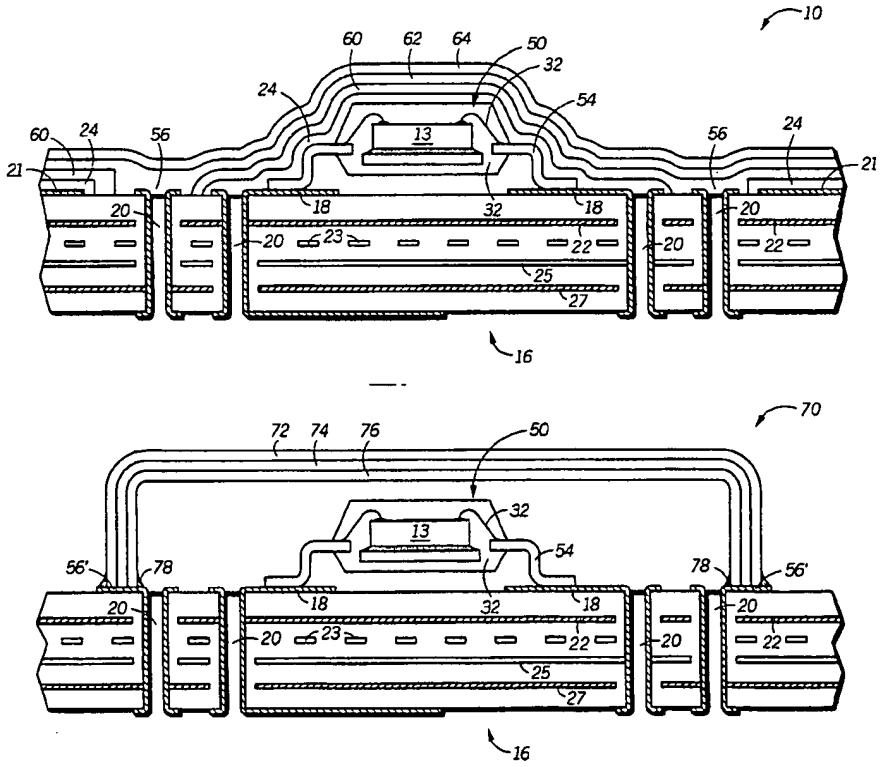
Primary Examiner—Laura Thomas

Attorney, Agent, or Firm—Patricia S. Goddard

[57] **ABSTRACT**

Electronic components are shielded from electromagnetic interference (EMI) by one or more conformal layers filled with selected filler particulars for attenuate specific EMI frequencies or a general range of frequencies. Shielding is accomplished through the use of a single general purpose shielding layer, or through a series of shielding layers for protecting more specific EMI frequencies. In a multilayer embodiment, a semiconductor device (**50**) is mounted on a printed circuit board substrate (**16**) as a portion of an electronic component assembly (**10**). A conformal insulating coating (**24**) is applied over the device to provide electrical insulation of signal paths (e.g. leads **54** and conductive traces **18**) from subsequently deposited conductive shielding layers. One or more shielding layers (**60**, **62**, and **64**) are deposited, and are in electrical contact with a ground ring (**56**). In a preferred embodiment, the ground connections for the shield layers are separate from those used for power distribution within the devices.

27 Claims, 7 Drawing Sheets



PATENT ABSTRACTS OF JAPAN

(11)Publication number : **11-307983**

(43)Date of publication of application : **05.11.1999**

(51)Int.Cl. **H05K 9/00**
H01L 23/29
H01L 23/31

(21)Application number : **10-128140**

(22)Date of filing : **21.04.1998**

(71)Applicant : **TOKIN CORP**

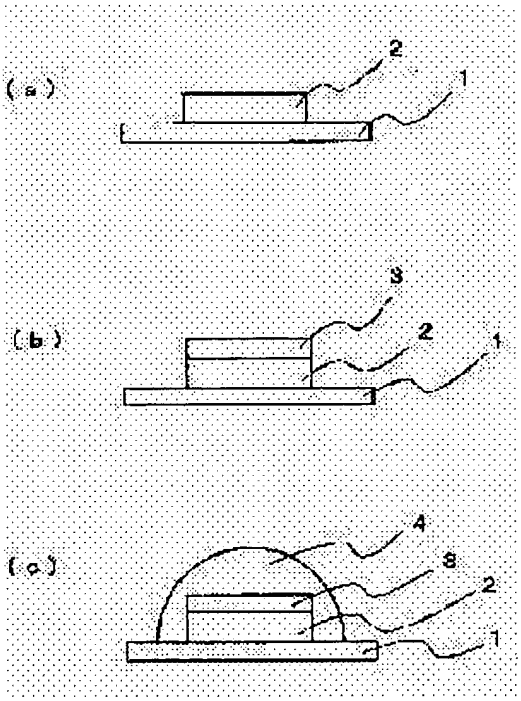
(72)Inventor : **KAMEI KOJI**
SATO MITSUHARU

(54) ELECTRONIC COMPONENT AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To make adaptable to working processes requiring the heat resistance by fixing an electromagnetic interference suppressor covered with a thermosetting resin to a semiconductor component or wiring board.

SOLUTION: An electromagnetic interference suppressor 3 is mounted so as to cover the top face of a semiconductor component 2 being a noise source disposed on the top of a wiring board 1 mounting CPU etc., and has a compsn. composed of a flat soft magnetic powder of Fe-Al-Si alloy 90 wt. parts, organic binder composed of a polyurethane resin 8 wt. parts and hardening agent 2 wt. parts and solvent 40 w. part. A thermosetting resin such as phenol resin, epoxy resin, etc., is coated so as to cover the entire surface of the electromagnetic interference suppressor 3, set, and hardened by a soldering reflow process to perfectly seal and fix the electromagnetic interference suppressor 3. Thus it is possible to improve the apparent heat resistance, without deteriorating its characteristics.



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